What Is Claimed Is:

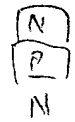
1. A non-volatile semiconductor memory comprising:

a semiconductor substrate having active and field regions;

at least two non-volatile storage transistors each having a storage at the active region and a control gate at the storage, wherein each control gate is incorporated into a single control plate; and

at least two selection transistors each of which corresponds to each non-volatile storage transistor, wherein each of the selection transistors is connected to the corresponding non-volatile storage transistors for selecting the corresponding non-volatile storage transistors.

2. The memory of claim 1, wherein the semiconductor substrate is a triple well type having an N-type well on a P-type substrate and a P-type well in the N-type well, wherein each of the active regions is formed in the P-type well.



3. The memory of claim 1, wherein the selection transistor is connected in series to the non-volatile storage transistor

through a PN-junction shared by the selection and non-volatile storage transistors.

4. The memory of claim 1, wherein the selection transistor is connected in series to the non-volatile storage transistor through a common channel.

5. The memory of claim 1, further comprising a plurality of dielectric layers at the non-volatile storage and the selection transistors, wherein each dielectric layer is formed of different materials or has different thickness.

6. The memory of claim 1, wherein the storage is a conductive floating gate.

7. The memory of claim 5, wherein the dielectric layers at the non-volatile storage transistors are formed of a tunneling oxide.

8. The memory of claim 1, further comprising:

a first dielectric layer between the storage and the substrate; and

a second dielectric layer between the substrate and the selection gate.

9. The memory of claim 1, wherein each of the storage is formed of a conductor.

10. The memory of claim 1, wherein each of the storage is one of a nitride layer or a nitride/oxide layer.

11. The memory of claim 10, wherein each of the storage is formed on the non-volatile storage transistor only.

12. The memory of claim 1, wherein the storage is formed of a ferroelectric material.

13. The memory of claim 1, wherein the at least two non-volatile storage transistors have at least one common impurity region for a source or a drain in the substrate.

14. A non-volatile semiconductor memory comprising:

a semiconductor substrate having active and field regions;

a dielectric layer on the substrate;

at least two non-volatile storage transistors on the substrate, each non-volatile storage transistor including a source and a drain in the substrate, a storage over the active region, and a control gate at the storage, wherein each control gate is incorporated into a single control plate and the source is shared by adjacent non-volatile storage transistors as a common source; and

at least two selection transistors on the substrate, each selection transistor including a source and a drain in the substrate, a selection gate on the dielectric layer between the source and the drain, wherein the source of each of the selection transistors acts as the drain of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor.

15. The memory of claim 14, wherein each of the sources of the selection transistors includes first and second sources, wherein the second source is formed in the first source and a programming operation is carried out through the first source, the storage of the corresponding non-volatile storage transistor, and the dielectric layer, and an erasing operation is carried out through the second source, the storage, and the dielectric layer.

16. The memory of claim 15, wherein the programming operation is carried out using a hot carrier injection.

17. The memory of claim 14, wherein the dielectric layer includes a first portion having a first thickness between the storage and the semiconductor substrate and a second portion having a second thickness different from the first thickness between the selection gate and the semiconductor substrate.

18. A non-volatile semiconductor memory array, comprising:

a plurality of bit lines arranged in a column direction;

a plurality of word lines arranged in a row direction;

a plurality of source lines arranged in the row direction;

a plurality of control plate lines arranged in the row direction; and

a plurality of non-volatile memory cells between the lines, each of the non-volatile memory cells includes,

at least two non-volatile storage transistors each of which includes a source and a drain in a substrate, a drain formed in the substrate, a storage over the active region, and a control gate at the storage, wherein each control gate is incorporated into a control plate built in a single body and the source is shared by adjacent non-volatile storage transistors as a common source, and

at least two selection transistors each of which includes a source and a drain in the substrate, a selection gate on the dielectric layer between the source and drain so as to be isolated from the storage, wherein the source of each of the selection transistors is the drain of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor, and selection gates of the respective cells

are connected to the corresponding word lines in the row direction, the common source of a unit cell is connected to the corresponding source line extending in the row direction, the control plate is connected to the corresponding control plate line in the row direction, and the drain of the selection transistor in the cell is connected to the corresponding bit line.

19. The array of claim 18, wherein the control plate lines and word lines are formed of the same conductive materials as the control plate and the selection gate, respectively.

20. The array of claim 18, wherein the array is operated in a flash memory mode.

21. The array of claim 20, wherein the selection gate of an unselected non-volatile storage transistor in the array is applied with 0V, grounded or floated, and the selection gate of a selected non-volatile storage transistor is applied with Vcc~10V for a programming operation, the selection gate of the selected non-volatile storage transistor is applied with Vcc~7V for a reading operation, the control plate of the selected non-volatile

storage transistor is applied with (-)7V~10V, (-)13V~0V, and 0V~7V for the programming operation, an erasing operation, and the read operation, respectively, a drain of the selected non-volatile storage transistor is applied with 1V~6V and 0.5V~2V for the programming operation and the reading operation, respectively, the common source of the selected non-volatile storage transistor is applied with 0V~2V, 0V~13V and 0V~1.5V for the programming, erasing, and reading operations, respectively, and the substrate is a P-type substrate.

22. The array of claim 20, wherein the selection gate of an unselected non-volatile storage transistor is applied with 0V, grounded or floated, and the selection gate of a selected non-volatile storage transistor is applied with Vcc~10V, Vcc~7V, and 0V~13V for programming, reading, and erasing operations or the selection gate of the selected non-volatile storage transistor is floated for the erasing operation, the control plate of the selected non-volatile storage transistor is applied with (-)7V~10V, (-)13V~0V, and 0V~7V for the programming, erasing, and reading operations, respectively, the drain of the selected non-volatile storage transistor is applied with 1V~6V, 0.5V~2V for the programming and reading operations, respectively, the common

source of the selected non-volatile storage transistor is applied with 0V~2V, Vcc~13V, and 0V~1.5V for the programming, erasing, reading operations, respectively, or the common source of the selected non-volatile storage transistor is floated for the erasing operation, the substrate includes a P-type substrate, an N-type well formed in the P-type substrate, and a P-type well formed in the N-type well, 0V is always applied to the P-type substrate, (-)5V~0V and Vcc~13V are applied to the P-type well for the programming and erasing operations, respectively, and 0V is applied to the N-type well for the programming and reading operations, and Vcc~13V is applied to the N-type well for the erasing operation.

23. The array of claim 18, wherein the array operates in an EEPROM mode of a cell unit.

24. The array of claim 23, wherein a selection gate of an unselected cell is applied with 0V, 0~Vcc or float, and 0V for programming, erasing, and reading operations, respectively, the drain of the selection transistor for the unselected cell is applied with 0V or float for the erasing operation, the selection

gate of the selected cell is applied with Vcc~10V, Vcc~10V or 7V~15V, and Vcc~7V for the programming, erasing, and reading operations, respectively, the drain of the selection transistor for the selected cell is applied with 2V~7V, Vcc~10V or 7V~13V, and 0.5V~2V for the programming, erasing, and reading operations, respectively, the control plate of the selected cell is applied with (-)7V~10V, (-)10V~(-)3V or 0V, and 0V~7V for the programming, erasing, and reading operations, respectively, the common source for the selected cell is applied with 0V~2V, 0V or float, and 0V~1.5V for the programming, erasing, and reading operations, respectively, and the substrate is a P-type substrate.

25. The array of claim 23, wherein the selection gates of unselected and selected cells are applied with 0V and Vcc~10V for a programming operation, the control gate of the selected cell is applied with (-)7~10V, the drain of the selection transistor for the selected cell is applied with 1~6V, and the common source of the selected cell is applied with 0~2V for the programming operation, the substrate includes a P-type substrate, an N-type well in the P-type substrate, and a P-type well in the N-type well, 0V is always applied to the substrate, and (-)5V~0V and 0V

are applied to the P-type and N-type wells for the programming operation, respectively.

26. In a non-volatile semiconductor memory including at least two non-volatile storage transistors each of which including a source in the substrate, a drain in the substrate, a storage on the dielectric layer over the active region, and a control gate at the storage, at least two control gates incorporating into a control plate built in a single body, and at least two selection transistors each of which including a source in the substrate, a drain in the substrate, a selection gate on the dielectric layer between the source and the drain to be isolated from the storage, wherein the source of each of the selection transistors is the drain of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor, a method of operating the non-volatile semiconductor memory, comprising:

selecting one of the non-volatile storage transistors by turning on or off the respective selection transistors; and

programming the selected non-volatile storage transistor using a hot carrier injection method generating hot electrons from a channel of the selected non-volatile storage transistor.

27. The method of claim 26, wherein the hot carrier injection method includes one of a first method of applying a reverse bias between the source of the selected non-volatile storage transistor and the substrate, a second method of increasing a voltage of the control plate of the selected non-volatile storage transistor gradually from a low voltage, and a third method of combining the first and second methods.

28. The method of claim 26, further comprising:

monitoring a channel current of the selected non-volatile storage transistor for a voltage applied to the control plate of the selected non-volatile storage transistor; and

terminating a programming operation of the voltage applied to the control plate when the channel current reaches a reference current for the voltage.

29. The method of claim 26, further comprising:

monitoring a channel current of the selected non-volatile storage transistor for voltages applied successively to the control plate of the selected non-volatile storage transistor; and

terminating programming operations of the respective voltages applied to the control plate when the channel current reaches a reference current for the voltages applied to the control plate.

30. The method of claim 26, further comprising:

monitoring a channel current of the selected non-volatile storage transistor for voltages applied successively to the control plate of the selected non-volatile storage transistor; and

terminating programming operations of the respective voltages applied to the control plate when the channel current reaches a reference current for the voltages applied to the control plate, respectively.

31. The method of claim 26, further comprising:

selecting one of the non-volatile storage transistors by turning on a corresponding selection transistor for a reading operation; and

applying a constant or a variable voltage to the control plate of the selected non-volatile storage transistor.

32. The method of claim 26, wherein the selection gates of the unselected non-volatile storage transistors are applied with one of 0V, Vcc~13V, or float for an erasing operation.

33. The method of claim 26, wherein each of the bit lines crossing a selected source line is applied with a voltage equal to a source voltage when a reading or programming operation is carried out by applying the source voltage to the selected cell in order to apply the same voltage to the source and drain of the unselected cell to prevent a leakage current generated from an unselected turned-on cell sharing a word line of the selected cell.

34. A non-volatile semiconductor memory array including a plurality of bit lines arranged in a row direction, a plurality

of word lines arranged in a column direction, a plurality of source lines arranged in the row direction, a plurality of control plate lines arranged in the row direction, and a plurality of non-volatile memory cells between the lines, each of the non-volatile memory cells, comprising:

at least two non-volatile storage transistors each of which including a source, a drain, a storage, and a control gate at the storage, wherein at least two control gates are incorporated into one control plate built in a single body and the source of adjacent non-volatile storage transistors is a common source; and

at least two selection transistors each of which including a source, a drain, a selection gate between the source and the drain to be isolated from the storage, wherein the source of each of the selection transistors is the drain of a corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor, wherein the selection gates of the respective cells are connected to corresponding word lines in the column direction, the common source is connected to a corresponding source line extending in the row direction, the control plate is connected to a corresponding control plate line in the row

direction, and the drain of the selection transistor is connected to the corresponding bit line.

35. The array of claim 34, wherein the source of the selected non-volatile storage transistor is applied with a source voltage and a voltage equal to the source voltage is applied to the bit line connected to the drain of the selection transistor for an adjacent non-volatile storage transistor sharing the common source for a reading or programming operation.

36. A non-volatile semiconductor memory comprising:

a semiconductor substrate having active and field regions;

a dielectric layer on the semiconductor substrate;

at least two non-volatile storage transistors on the substrate each of which including a source in the substrate, a drain in the substrate, a storage on the dielectric layer over the active region, and a control gate at the storage, wherein at least two control gates are incorporated into a single control plate and the drain is shared by the adjacent non-volatile storage transistors as a common drain; and

at least two selection transistors on the substrate each of which including a source in the substrate, a drain in the substrate, a selection gate on the dielectric layer between the source and the drain to be isolated from the storage, wherein the drain of each of the selection transistors is the source of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor.

37. The memory of claim 36, wherein each of the drains of the selection transistors includes a first drain and a second drain in the first drain, wherein a programming operation is carried out through the first drain, the storage of the corresponding non-volatile storage transistor, and the dielectric layer, and an erasing operation is carried out through the second drain, the storage gate, and the dielectric layer.

38. The memory of claim 36, wherein the programming operation is carried out using a hot carrier injection.

39. The memory of claim 36, wherein the control plate has an opening at a central part to contact the common drain with the bit line.

40. The memory of claim 36, wherein the dielectric layer includes a first portion having a first thickness between the storage and the semiconductor substrate and a second portion having a second thickness different from the first thickness between the selection gate and the semiconductor substrate.

41. A non-volatile semiconductor memory array, comprising:

a plurality of bit lines arranged in a column direction;

a plurality of word lines arranged in a row direction;

a plurality of source lines arranged in the row direction;

a plurality of control plate lines arranged in the row direction; and

a plurality of non-volatile memory cells between the lines, each of the non-volatile memory cells including,

at least two non-volatile storage transistors each of which having a source formed in a substrate, a drain in the substrate,

a storage on the dielectric layer over the active region, and a control gate at the storage, wherein at least two control gates are incorporated into a single control plate and the drain is shared by adjacent non-volatile storage transistors as a common drain, and

at least two selection transistors each of which having a source in the substrate, a drain in the substrate, a selection gate on the dielectric layer between the source and the drain to be isolated from the storage, wherein the drain of each of the selection transistors is the source of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor, wherein the selection gates of the respective cells are connected to the corresponding word lines in the row direction, the common drain of a unit cell is connected to the corresponding bit line extending in the row direction, the control plate is connected to the corresponding control plate line in the row direction, and the source of the selection transistor in the cell is connected to the corresponding source line.

42. The array of claim 41, wherein the control plate lines and the word lines are formed of the same conductive materials as the control plate and the selection gate, respectively.

43. The array of claim 41, wherein the selection gate of the unselected non-volatile storage transistor is applied with 0V or is floated, the selection gate of the selected non-volatile storage transistor is applied with Vcc~10V for a programming operation, Vcc~7V for a reading operation, the control plate of the selected non-volatile storage transistor is applied with (-)7V~10V, one of (-)10V~(-)5V/0V/(-)10~(-)3V, and 0V~7V for the programming operation, an erasing operation, and the reading operation, respectively, the common drain of the selected non-volatile storage transistor is applied with 2V~7V and 0.5V~2V for the programming operation and the reading operation, respectively, the source of selection transistor for the selected non-volatile storage transistor is applied with Vs(0V~2V), Vcc~10V and Vs for the programming, erasing, and reading operations, respectively, and the substrate is a P-type substrate.

44. The array of claim 41, wherein the selection gate of the selected non-volatile storage transistor is applied with Vcc~10V, Vcc~7V, and 0V~Vpp(Vcc~13V) for programming, reading, and erasing operations, respectively, or is floated for the erasing operation, the control plate of the selected non-volatile storage transistor is applied with (-)7V~10V, (-)13V~0V, and 0V~7V for the programming, erasing, and reading operations, respectively, the common drain of the selected non-volatile storage transistor is applied with 1V~6V and 0.5V~2V for the programming and reading operations, respectively, the source of the selection transistor for the selected non-volatile storage transistor is applied with Vs(0V~2V), Vpp or float, and Vs for the programming, erasing, and reading operations, respectively, and the substrate includes a P-type substrate, an N-type well in the P-type substrate, and a P-type well in the N-type well, 0V is always applied to the P-type substrate, (-)5V~0V and Vpp are applied to the P-type well for the programming and erasing operations, respectively, and 0V and Vpp are applied to the N-type well for the programming and erasing operations, respectively.

45. A non-volatile semiconductor memory, comprising:

a semiconductor substrate having active and field regions;

a dielectric layer on the semiconductor substrate;

at least two non-volatile storage transistors each of which including a source in the substrate, a drain in the substrate, a storage on the dielectric layer over the active region, and a control gate at the storage, wherein at least two control gates are incorporated into a single control plate; and

at least two selection transistors each of which including a source in the substrate, a drain in the substrate, a selection gate on the dielectric layer between the source and the drain to be isolated from the storage, wherein the drain of each of the selection transistors acts as the source of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistors.

46. The memory of claim 45, wherein the dielectric layer includes a first portion having a first thickness between the storage and the semiconductor substrate and a second portion

having a second thickness different from the first thickness between the selection gate and the semiconductor substrate.

47. A non-volatile semiconductor memory array, comprising:

a plurality of bit lines arranged in a row direction;

a plurality of word lines arranged in a column direction;

a plurality of source lines arranged in the row direction;

a plurality of control plate lines arranged in the row direction; and

a plurality of non-volatile memory cells between the lines, each of the non-volatile memory cells including,

at least two non-volatile storage transistors each of which having a source in a substrate, a drain formed in the substrate, a storage on the dielectric layer over the active region, and a control gate at the storage, wherein at least two control gates are incorporated into a single control plate; and

at least two selection transistors each of which having a source in the substrate, a drain in the substrate, a selection gate on the dielectric layer between the source and the drain to be isolated from the storage, wherein the drain of each of the

selection transistors is the source of the corresponding non-volatile storage transistor, and each of the two selection transistors is connected to the corresponding non-volatile storage transistor for selecting the corresponding non-volatile storage transistor, wherein the selection gates of the respective cells are connected together to the corresponding word lines in the column direction, the drains of the cells are connected to the different bit lines, the control plate is connected to the corresponding control plate line in the row direction, and the source of the selection transistor is connected to the corresponding source line.

48. A non-volatile memory comprising:

a semiconductor substrate having active and field regions;

a dielectric layer on the semiconductor substrate;

a first source in the active region;

a common drain in the active region to have a first channel between the common drain and the first source;

a second source in the active region to have a second channel between the common drain and the second source;

a first gate and a first storage on the dielectric layer in parallel with each other over the first channel;

a second gate and a second storage on the dielectric layer in parallel with each other over the second channel; and

a control plate built in a single body over the first and second storage.

49. The memory of claim 48, wherein the control plate has an opening at a central part to contact the common drain with a bit line.

50. A non-volatile semiconductor memory array comprising:

a plurality of bit lines arranged in a column direction;

a plurality of word lines arranged in a row direction;

a plurality of source lines arranged in the row direction;

a plurality of control plate lines arranged in the row direction; and

a plurality of non-volatile memory cells between the lines, each of the non-volatile memory cells including,

a semiconductor substrate having active and field regions;

a dielectric layer on the semiconductor substrate;

a first source in the active region;

a common drain in the active region to have a first channel between the common drain and the first source;

a second source in the active region to have a second channel between the common drain and the second source;

a first gate and a first storage on the dielectric layer in parallel with each other over the first channel;

a second gate and a second storage on the dielectric layer in parallel with each other over the second channel; and

a control plate built in a single body over the first and second storage,

wherein the first storage, the common drain, and the control plate form a first non-volatile storage transistor, the first source and the selection gate form a first selection transistor for the first non-volatile storage transistor, the second storage, the common drain, and the control plate form a second non-volatile storage transistor, and the second source and the selection gate form a second selection transistor for the second non-volatile storage transistor, and

wherein the selection gates of the cell are connected to the different corresponding word lines, the common drain is connected to the corresponding bit lines, the control plate is connected to the corresponding control plate lines, and the sources of the selection transistors of the cell are connected to the different source lines.

51. The array of claim 50, wherein the selected common drain is applied with 2V~8V in a programming operation, the control plate of the selected non-volatile storage transistor is applied with (-)5V~10V, a voltage higher than that of a threshold voltage of the selection transistor is applied to the selection gate of the selected selection transistor, and 0~2V lower than the common drain voltage is applied to the source of the selected selection transistor.

52. The array of claim 50, wherein the selection gate of the selected selection transistor is applied with 0V for an erasing operation, the control plate of the selected non-volatile storage transistor is applied with (-)10V~(-)5V or 0V, and the common drain is applied with 0V~8V or 8V~(-)13V.

53. The array of claim 50, wherein the selection gate of the selected selection transistor is applied with Vcc~20V and the control plate of the selected non-volatile storage transistor is applied with (-)8V~0V for an erasing operation.

54. A non-volatile memory comprising:

a first conductive type semiconductor substrate having active and field regions;

a first region in the active region, the first region having a second conductive type;

a second region having the second conductive type to have a first channel between the first and second regions;

a third region having the second conductive type to have a second channel between the second and third regions;

a first non-volatile storage on the first channel to be overlapped at least a portion of the second region;

a first dielectric between the substrate and the first non-volatile storage;

a second non-volatile storage on the second channel to be overlapped at least a portion of the second region;

a second dielectric between the substrate and second non-volatile storage;

a first selection gate over the first channel to be overlapped at least a portion of the first region;

a third dielectric between the first selection gate and substrate;

a fourth dielectric between the first non-volatile storage and first selection gate;

a second selection gate over the second channel to be overlapped at least a portion of the third region;

a fifth dielectric between the second selection gate and the substrate;

a sixth dielectric between the second non-volatile storage and the second selection gate;

a control plate over the first and second non-volatile storage, the control plate built in a single body; and

a seventh dielectric between the control plate and the non-volatile storage.

55. The non-volatile semiconductor memory of claim 54, wherein at least two of the first to seventh dielectrics are formed to the same thickness and the same material.

56. The non-volatile semiconductor memory of claim 54, wherein the non-volatile storage is a floating gate.

57. The non-volatile semiconductor memory of claim 54, wherein the non-volatile storage is formed of one of a nitride layer and a stacked nitride/oxide layer.

58. The non-volatile semiconductor memory of claim 54, wherein the first and second conductive types are P and N, respectively.

59. The non-volatile semiconductor memory of claim 54, wherein the first and third regions are sources and the second region is a common drain.

60. The non-volatile semiconductor memory of claim 54, wherein the selection gate is formed of polysilicon and acts as a spacer.

61. The non-volatile semiconductor memory of claim 54, wherein the control plate has an opening to contact a bit line with the second region.

62. The non-volatile semiconductor memory of claim 61, further comprising a plug between the first and second non-volatile storage, formed of the same material as the selection gates, electrically contacted with the second region through the opening, and electrically isolated from the non-volatile storage and control plate.

63. The non-volatile semiconductor memory of claim 62, wherein the selection gates and plug are formed by anisotropic etch.

64. The non-volatile semiconductor memory of claim 54, further comprising an insulating spacer at a lateral side of the control plate.

65. The non-volatile semiconductor memory of claim 54, wherein the first and second non-volatile storage are thicker than the selection gates.

66. The non-volatile semiconductor memory of claim 54, wherein the selection gate has a thickness greater than an added thickness of the non-volatile storage and the control plate.

67. A memory device having a plurality of memory cells in first and second directions to form an array of memory cells, the memory cell having at least one operating mode for at least one of programming, erasing and reading of the memory cells, wherein the improvement comprises:

each memory having a first transistor with a control gate and a storage gate and a second transistor having a selection

gate, wherein a pair of adjacent memory cells commonly share a plate line as the control gate of the first transistor.

68. The memory device of claim 67, wherein the storage gate comprises at least one of polysilicon, metal, silicide, ferroelectric layer and a dielectric.

69. The memory device of claim 67, wherein the first transistor of each memory further includes first and second electrodes and the second transistor of each memory cell further includes first and second electrodes, the second electrode of the first transistor is commonly coupled to the first electrode of the second transistor.

70. The memory device of claim 69, wherein a word line coupled to the selection gate, a control plate line coupled to the plate line, a first electrode line coupled to the first electrode of first transistor is formed in a first direction, and a bit line coupled to the second electrode of the second transistor is formed in a second direction.

71. The memory device of claim 69, wherein a bit line coupled to the second electrode of the second transistor, a control plate line coupled to the plate line, a first electrode line coupled to the first electrode of first transistor is formed in a first direction, and a word line coupled to the selection gate is formed in a second direction.

72. The memory device of claim 69, wherein a word line coupled to the selection gate, a control plate line coupled to the plate line, and a first electrode line coupled to the second electrode of the second transistor is formed in a first direction, and a bit line coupled to the first electrode of first transistor is formed in a second direction.

73. The memory device of claim 67, wherein the first transistor of each memory further includes first and second electrodes and the second transistor of each memory cell further includes first and second electrodes, the second electrode of the first transistor being commonly coupled to the first electrode of the second transistor and the first electrode of the first transistors in the pair of adjacent memory cells is commonly coupled to each other.

74. The memory device of claim 67, wherein the control gate and the storage gate are formed in a split gate structure.

75. The memory device of clam 74, wherein the second transistor includes a first electrode and the first transistor includes a second electrode, a source line coupled to the first electrode, a word line coupled to the selection gate, and a control plate line being coupled to the plate line being formed in the first direction, and a bit line coupled to the second electrode of the first transistor being formed in the second direction.

76. The memory device of claim 75, wherein the second electrode of the first transistors in the pair of adjacent memory cells is commonly coupled to each other.